

1-39-L3

Designer's Data Sheet
Power Field Effect Transistor
N-Channel Enhancement-Mode
Silicon Gate TMOS

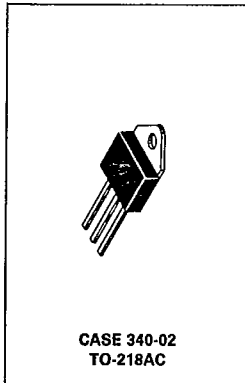
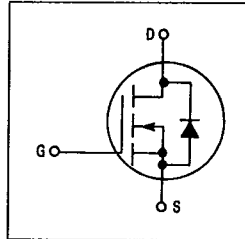


These TMOS Power FETs are designed for high voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designer's Data — I_{DSS} , $V_{DS(on)}$, $V_{GS(th)}$ and SOA Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads

MTH15N35
MTH15N40

TMOS POWER FETs
 15 AMPERES
 $r_{DS(on)} = 0.3 \text{ OHM}$
 350 and 400 VOLTS



MAXIMUM RATINGS

Rating	Symbol	MTH		Unit
		15N35	15N40	
Drain-Source Voltage	V_{DSS}	350	400	Vdc
Drain-Gate Voltage ($R_{GS} = 1 \text{ M}\Omega$)	V_{DGR}	350	400	Vdc
Gate-Source Voltage	V_{GS} V_{GSM}	± 20 ± 40		Vdc
Continuous				Vpk
Non-repetitive ($t_p \leq 50 \mu s$)				
Drain Current — Continuous	I_D	15		Adc
— Pulsed	I_{DM}	75		
Total Power Dissipation @ $T_C = 25^\circ C$	P_D	150		Watts
Derate above 25°C		1.2		W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	-65 to 150		°C

THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case	$R_{\theta JC}$	0.83	°C/W
— Junction to Ambient	$R_{\theta JA}$	30	
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 5 seconds	T_L	275	°C

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ C$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Drain-Source Breakdown Voltage ($V_{GS} = 0, I_D = 0.25 \text{ mA}$)	$V_{(BR)DSS}$	350 400	—	Vdc
Zero Gate Voltage Drain Current ($V_{DS} = \text{Rated } V_{DSS}, V_{GS} = 0$)	I_{DSS}	—	0.2 1	mAdc
($V_{DS} = 0.8 \text{ Rated } V_{DSS}, V_{GS} = 0, T_J = 125^\circ C$)				
Gate-Body Leakage Current, Forward ($V_{GSF} = 20 \text{ Vdc}, V_{DS} = 0$)	I_{GSSF}	—	100	nAdc
Gate-Body Leakage Current, Reverse ($V_{GSR} = 20 \text{ Vdc}, V_{DS} = 0$)	I_{GSSR}	—	100	nAdc

(continued)

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS — continued ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit	
ON CHARACTERISTICS*					
Gate Threshold Voltage ($V_{DS} = V_{GS}$, $I_D = 1\text{ mA}$) $T_J = 100^\circ\text{C}$	$V_{GS(th)}$	2 1.5	4.5 4	Vdc	
Static Drain-Source On-Resistance ($V_{GS} = 10\text{ Vdc}$, $I_D = 8\text{ Adc}$)	$r_{DS(on)}$	—	0.3	Ohm	
Drain-Source On-Voltage ($V_{GS} = 10\text{ V}$) ($I_D = 15\text{ Adc}$) ($I_D = 8\text{ Adc}$, $T_J = 100^\circ\text{C}$)	$V_{DS(on)}$	—	4.5 3.5	Vdc	
Forward Transconductance ($V_{DS} = 10\text{ V}$, $I_D = 8\text{ A}$)	g_{FS}	5	—	mhos	
DYNAMIC CHARACTERISTICS					
Input Capacitance	$(V_{DS} = 25\text{ V}$, $V_{GS} = 0$, $f = 1\text{ MHz}$) See Figure 11	C_{iss}	—	3000	pF
Output Capacitance		C_{oss}	—	500	
Reverse Transfer Capacitance		C_{res}	—	200	
SWITCHING CHARACTERISTICS* ($T_J = 100^\circ\text{C}$)					
Turn-On Delay Time	$(V_{DD} = 25\text{ V}$, $I_D = 0.5\text{ Rated } I_D$ $R_{gen} = 50\text{ ohms}$) See Figures 13 and 14	$t_{d(on)}$	—	60	ns
Rise Time		t_r	—	180	
Turn-Off Delay Time		$t_{d(off)}$	—	450	
Fall Time		t_f	—	180	
Total Gate Charge	$(V_{DS} = 0.8\text{ Rated } V_{DSS}$, $I_D = \text{Rated } I_D$, $V_{GS} = 10\text{ V}$) See Figure 12	Q_g	110 (Typ)	160	nC
Gate-Source Charge		Q_{gs}	50 (Typ)	—	
Gate-Drain Charge		Q_{gd}	60 (Typ)	—	
SOURCE DRAIN DIODE CHARACTERISTICS*					
Forward On-Voltage	$(I_S = \text{Rated } I_D$ $V_{GS} = 0)$	V_{SD}	1.3 (Typ)	1.6	Vdc
Forward Turn-On Time		t_{on}	Limited by stray inductance		
Reverse Recovery Time		t_{rr}	1200 (Typ)	—	ns
INTERNAL PACKAGE INDUCTANCE					
Internal Drain Inductance (Measured from screw on tab to center of die) (Measured from the drain lead 0.25" from package to center of die)	L_d	4 (Typ) 5 (Typ)	—	—	nH
Internal Source Inductance (Measured from the source lead 0.25" from package to center of die)	L_s	10 (Typ)	—	—	

*Pulse Test: Pulse Width $\leq 300\ \mu\text{s}$, Duty Cycle $\leq 2\%$.

TYPICAL ELECTRICAL CHARACTERISTICS

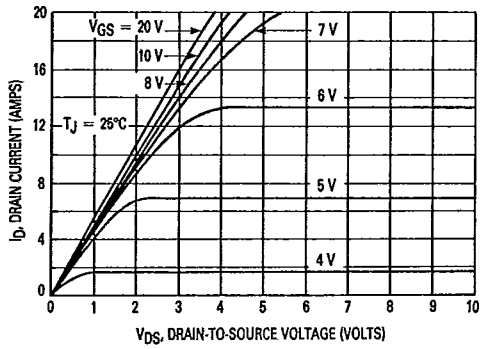


Figure 1. On-Region Characteristics

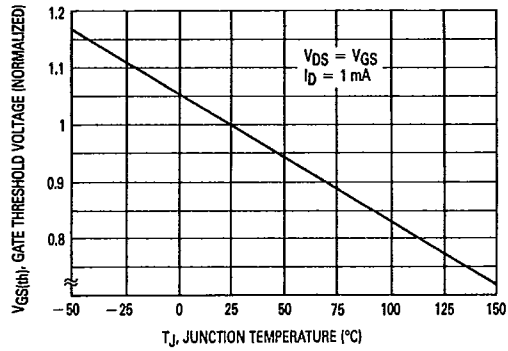


Figure 2. Gate-Threshold Voltage Variation With Temperature

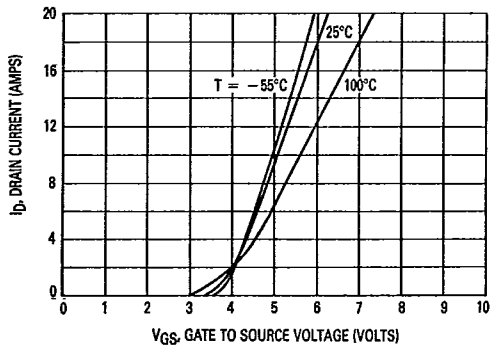


Figure 3. Transfer Characteristics

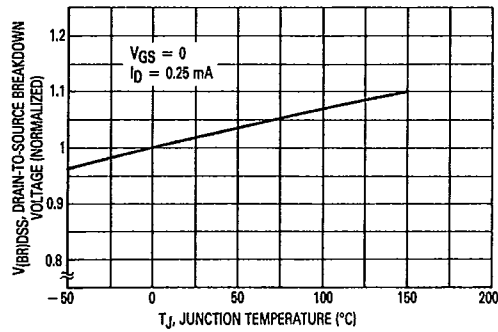


Figure 4. Breakdown Voltage Variation With Temperature

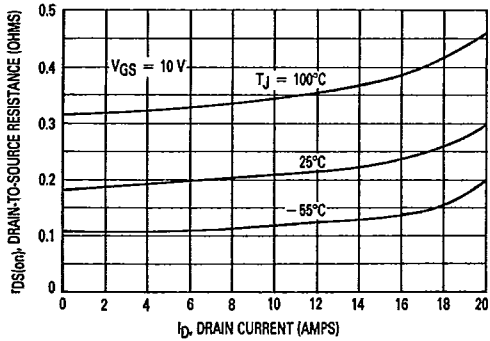


Figure 5. On-Resistance versus Drain Current

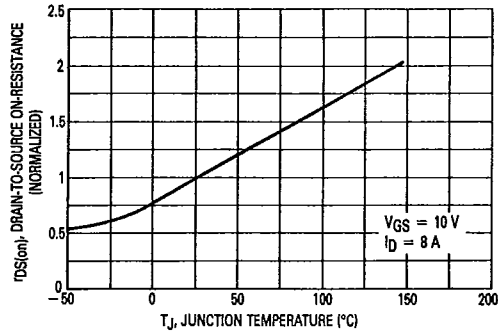


Figure 6. On-Resistance Variation With Temperature

SAFE OPERATING AREA INFORMATION

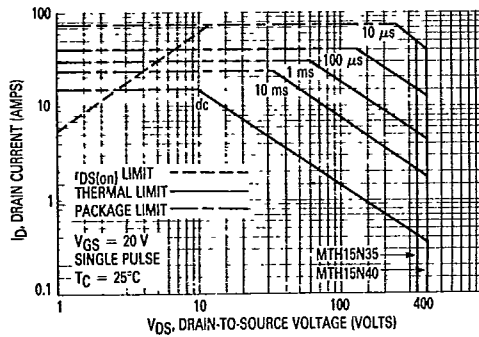


Figure 7. Maximum Rated Forward Biased Safe Operating Area

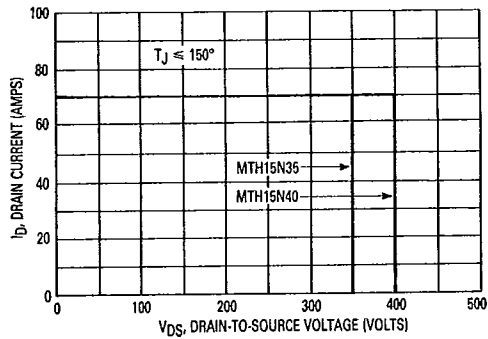


Figure 8. Maximum Rated Switching Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_J(\max) - T_C}{R_{\theta JC}}$$

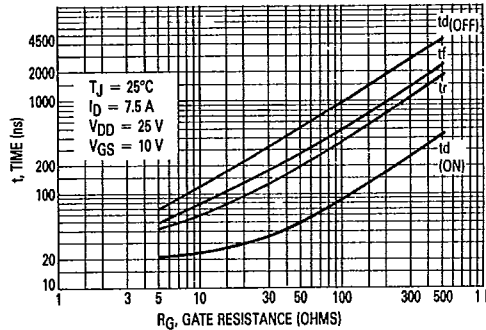


Figure 9. Resistive Switching Time Variation versus Gate Resistance

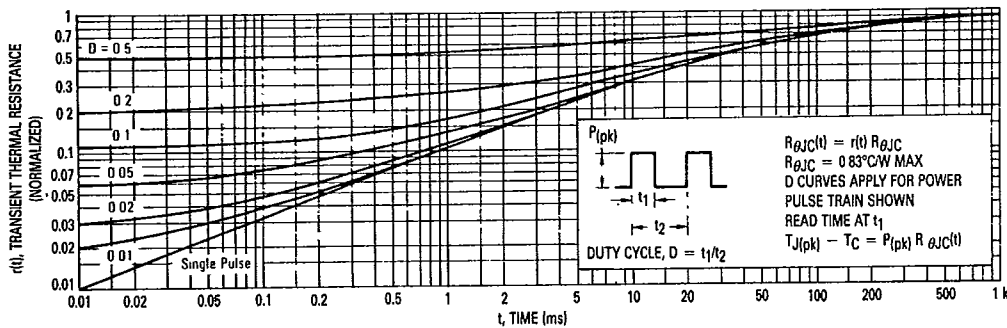


Figure 10. Thermal Response

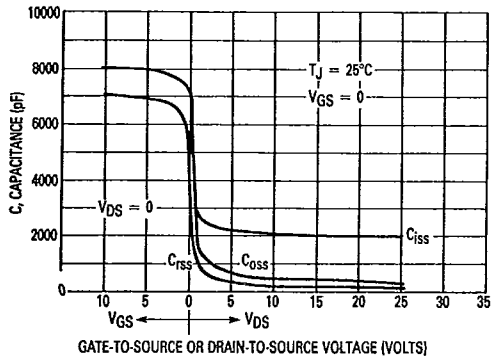


Figure 11. Capacitance Variation

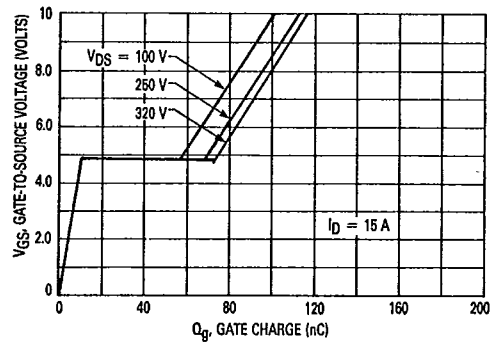


Figure 12. Gate Charge versus Gate-to-Source Voltage

RESISTIVE SWITCHING

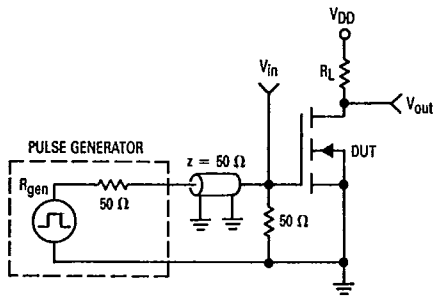


Figure 13. Switching Test Circuit

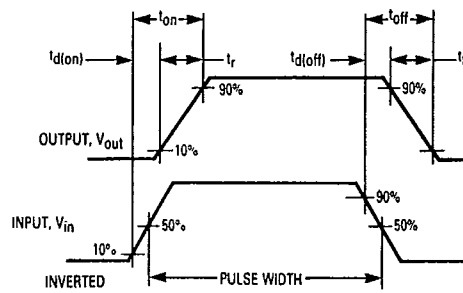
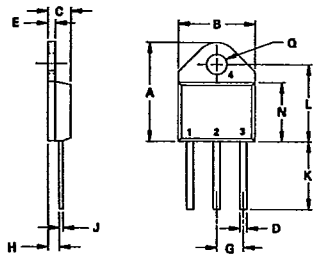


Figure 14. Switching Waveforms

OUTLINE DIMENSIONS

CASE 340-02
TO-218AC



STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	20.32	21.08	0.800	0.830
B	15.49	15.90	0.610	0.626
C	4.19	5.08	0.165	0.200
D	1.02	1.65	0.040	0.065
E	1.36	1.65	0.053	0.065
G	5.21	5.72	0.205	0.225
H	2.65	2.94	0.104	0.116
J	0.51	0.71	0.020	0.028
K	12.70	15.49	0.500	0.610
L	15.88	16.51	0.625	0.650
N	12.19	12.70	0.480	0.500
Q	4.64	4.22	0.159	0.166